Top-Down Fabrication of Sub-30 nm Monocrystalline Silicon Nanowires Using Conventional Microfabrication

Songyue Chen,[†,‡,§] Johan G. Bomer,[†,§] Wilfred G. van der Wiel[‡,§] Edwin T. Carlen,[†,§,*] and Albert van den Berg[†,§]

[†]BIOS Lab on a Chip Group, [‡]NanoElectronics Group, and [§]MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands

ABSTRACT We report a new low-cost top-down silicon nanowire fabrication technology requiring only conventional microfabrication processes including microlithography, oxidation, and wet anisotropic plane-dependent etching; high quality silicon nanowire arrays can be easily made in any conventional microfabrication facility without nanolithography or expensive equipment. Silicon nanowires with scalable lateral dimensions ranging from 200 nm down to 10—20 nm and lengths up to ~100 μm can be precisely formed with near-perfect monocrystalline cross sections, atomically smooth surfaces, and wafer-scale yields greater than 90% using a novel size reduction method where silicon nanowires can be controllably scaled to any dimension and doping concentration independent of large contacting regions from a continuous layer of crystalline silicon.

KEYWORDS: silicon nanowire · top-down nanofabrication · site binding model · biosensing

Over the past decade, there has been increasing interest in semiconductor nanowires due to their unique electrical, mechanical, and optical properties,[1−4] especially for label-free biosensing;[5−11] however, device and technology development have been limited to a small number of research laboratories typically relying on expensive nanolithography or specialized equipment and processes.[11−18] In general, research over the past five decades has resulted in a large number of nanofabrication techniques and equipment for nanodevice realization with unprecedented precision, largely fueled by the semiconductor industry's need for ultra-high density semiconductor circuits and systems. The silicon nanowire (Si-NW) nanofabrication toolbox consists of techniques that can be broadly classified as either bottom-up or top-down. Bottom-up nanofabrication is in principle simple and provides many high quality materialsl; however, suitable methods for accurate nanowire alignment are lacking, and electrical contact formation is problematic, making it difficult to construct functional device arrays.[18] Several key advantages favoring top-down Si-NW nanofabrication include well-established techniques for nanopatterning, semiconductor doping, electrical contact formation, and, very importantly, the commercial availability of high quality silicon-on-insulator (SOI) substrates. Conventional top-down nanopatterning techniques, such as deep-UV[9] and immersion deep-UV photolithography are currently the standard for semiconductor manufacturing; however, these techniques are extremely expensive and accessible only to large-scale integrated circuit manufacturers. Advanced nanopatterning, such as electron beam lithography and focused-ion-beam lithography can write feature sizes below 10 nm; however, serial patterning is not practical for wafer-scale fabrication and equipment and operation is typically expensive. More recently, Si-NW arrays with 15 nm lateral dimensions have been realized with nanoimprint lithography;[14] however, the replication stamp fabrication is complicated and wafer-level patterning remains problematic.

We present a new simple Si-NW fabrication technology that requires only two microlithography steps and conventional microfabrication processes on SOI wafers to form long (ranging from a few micrometers up to ~100 μm) Si-NWs with scalable lateral dimensions ranging from 200 nm down to 10−20 nm with near-perfect crystalline cross sections, atomically smooth surfaces, and wafer-scale yields greater than 90% using a novel size reduction method where nanowires can be controllably scaled to any dimension and doping concentration, independent of large contacting regions, from a continuous layer of crystalline silicon. Extensive electrical and electrochemical measurement results, as well as a discussion of device physics and operation, are presented.

*Address correspondence to e.t.carlen@utwente.nl.

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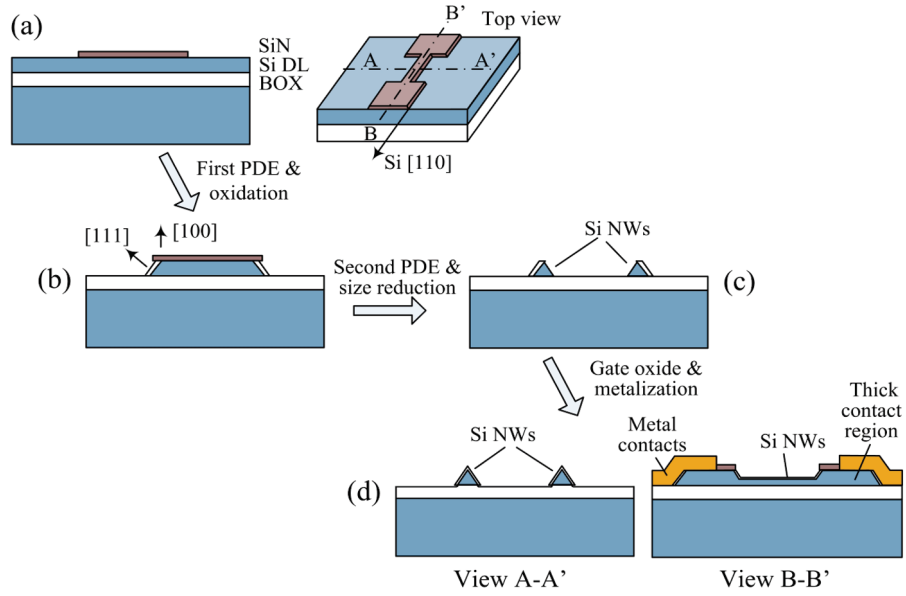

Figure 1. Top-down Si-NW microfabrication procedure (not to scale): (a) first lithography and etch steps for SiN layer patterning (BOX: buried oxide layer and Si DL: silicon device layer of the SOI substrate); (b) silicon device layer PDE and local oxidation; (c) second PDE and size reduction; (d) gate oxidation and contact metalization.

RESULTS AND DISCUSSION

The new Si-NW fabrication technology is shown in the brief process sequence of Figure 1. The Si-NW channel conductivity is selectively controlled using conventional shallow ion-implantation to eliminate implant-induced crystal damage. A thin silicon nitride (SiN) layer is first patterned on the silicon device layer along the [110] direction, which is a mask for the first plane-dependent wet etching (PDE) step (Figure 1a). The (100) planes etch 5−10 times faster than the (111) planes in an alkaline etchant, resulting in a trapezoidal silicon region with precisely defined sidewall angles (~54.7°), due to the intersection of the (100) and (111) planes. The exposed (111) facets are then thermally oxidized, which results in a small lateral, or localized, silicon oxidation at the Si/SiN interface (Figure 1b). The localized oxide layer protects the top edge of the Si-NW from void formation that has been reported for other masking layers.[11,19,20]

A second lithography step is used to pattern and etch the SiN mask layer again and a second PDE step forms the Si-NWs with isosceles triangular cross sections (Figure 1c) where the base (100) plane is in contact with the buried oxide layer and the (111) planes form the upper surfaces. It should be noted that the (111) silicon planes are ideally suited for direct organic monolayer formation, which is important for biological interfacing applications, such as biosensing. The Si-NW dimensions can be further reduced as desired (Figure 1d) using a simple and controllable method for selective size-reduction while the contact regions remain the same thickness as the original silicon device layer, thus integrating macroscale electrical interconnects with nanoscale device regions from a continuous layer of single crystal silicon (Figure 1d). Although the local oxidation method has been previously reported for the fabrication of Si-NWs,[21] we present significant new advances including conformal masking, selective size reduction, and defect-free ion-implantation impurity doping, and a continuous silicon layer connecting the NWs to microscale electrical contact regions, which facilitates reliable low resistance electrical contacts (see Supporting Information).

Figure 2 shows multiscale microscopy images representative of Si-NWs fabricated with this technology. Currently our test dies have about 200 Si-NWs devices (Figure 2a); however, this fabrication technology is capable of producing high-density Si-NW arrays with device diameters down to 10−20 nm and pitches ~50−60 nm with the use of high resolution patterning methods to define the initial SiN masking layer (Figure 1a). However, the majority of applications do not require ultrahigh density device arrays. The multiscale microscopy images clearly demonstrate the remarkable effectiveness of this fabrication technology for manufacturing high quality functional Si-NW devices and arrays with well-controlled sub-30 nm lateral dimensions, smooth (111) surfaces, and high wafer-level yield using only conventional microfabrication processes (see Supporting Information, Figure S4).

The combination of three key fabrication steps facilitate this new Si-NW fabrication technology, including PDE, localized silicon oxidation, and size reduction etching resulting in the new size-reduced recessed Si-NWs; details of these key process steps are now described in more detail.

Crystal plane dependent processes on silicon surfaces have been known for more than 50 years[22] and have profound effects on the behavior of reactive processes, such as PDE.[23−25] The different crystal planes etch anisotropically by hydroxide ions in alkaline solutions where (111) planes have one dangling bond per unit cell and have the lowest etch rate and the (100) and (110) planes both have two dangling bonds per unit cell and have higher etch rates[24] (see Supporting Information). Using this technique, we have been able to pattern Si-NWs with lengths up to 100 μm resulting in ratios of the lateral dimensions to length dimensions of more than 10^4.

The local oxidation of silicon at the Si/SiN interface has been well studied[26] and the lateral oxidation in the *x*-direction (Figure 3) provides a uniform oxide protection layer along the *z*-direction on the silicon surface

that facilitates the formation of Si-NWs with large aspect ratios (>10^4). The local oxidation results from the lateral diffusion of oxidant and subsequent reaction with the silicon, which produces a volumetric expansion of the SiO_2 interface layer that vertically displaces the SiN masking layer and produces the well-known "bird's beak" effect shown in Figure 3, the result of a two-dimensional finite-element numerical simulation (Taurus TSuprem-4, Synopsis). The lateral oxidation distance *l* is strongly dependent on the initial oxide thickness between the SiN and silicon device layer *d*;[26] for example, an oxide thickness of $d = 1$ nm results in a lateral oxide growth of $l \approx 20$ nm (see Supporting Information).

The most common top-down Si-NW fabrication approach is to first reduce the silicon device layer thickness, followed by nanopatterning and subsequent pattern transfer to form the Si-NW. However, thin electrical contact regions can lead to high contact resistances[18] and conventional doping methods can be difficult to control. Using the silicon dioxide from the initial oxidation step (Figure 1b) as a protection layer, the exposed (111) silicon planes continue to etch in a controllable way with an average etch rate of ~24 nm/min (see Supporting Information, Figure S3). The oxidized surface of the Si-NW prevents etching of the (100) planes, because all dangling silicon bonds have been terminated with oxygen from the thermal oxidation step (Figure 4a) and only nonoxidized dangling silicon bonds react with the hydroxide ions. The exact number of atoms at the apex of the size-reduced Si-NWs is not known; however, HRTEM images of size reduced Si-NWs show a relatively sharp transition at the intersection of the (111) and ($\bar{1}$11) planes (Figure 4a). The Si-NW width can be precisely determined from height measurements (with TMAFM) using $w \approx 2h/\tan(54.7°)$.

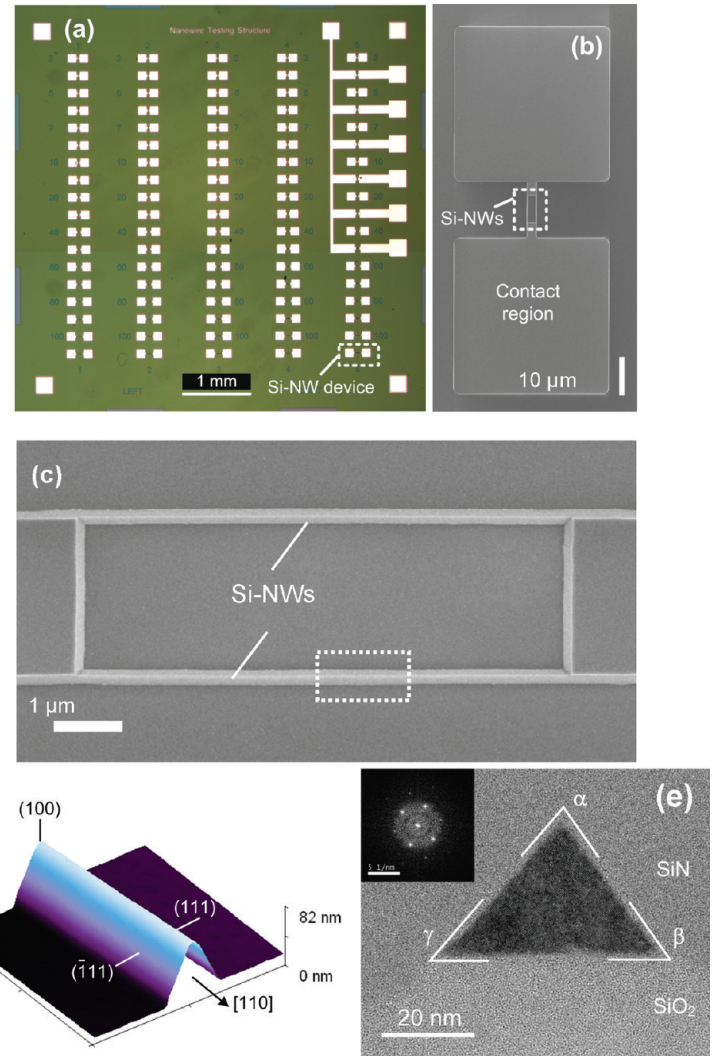

Figure 2. Multiscale microscopy images of fabricated Si-NWs: (a) optical microscopy image of a die (bright regions are aluminum contact metal); (b) high-resolution scanning electron microscopy (HRSEM) image showing electrical contact pad regions and two centrally located Si-NWs indicated with dashed white rectangle; (c) HRSEM of triangular Si-NWs; (d) tapping-mode atomic force microscopy (TMAFM) image of single Si-NW (NW height: 60 nm); (e) high resolution transmission electron microscopy (HRTEM) image of monocrystalline Si-NW cross-section with angles α = 77°, β = 54.7°, and γ = 48°. Inset: diffraction pattern indicates [011] zone axis along the device length.

A key advantage of this new size reduction method is that the electrical contact regions are not reduced in thickness, thus providing reliable low-resistance contacts, and the Si-NW device regions are recessed to the desired dimensions in a thin silicon region (Figure 4b). Another benefit of this new size reduction method is the removal of the initial shallow ion-implantation region eliminating crystal damage in the Si-NW channel.

High-resolution TEM cross sections (Figure 2e) of a representative Si-NW show monocrystalline silicon and the accompanying diffraction patterns (Figure 2e, inset) indicate that the [011] crystal direction lies along the device length as expected. The measured intersection angles between the (111) and (100) planes are $\alpha \approx 77°$, $\beta \approx 54.7°$, and $\gamma \approx 48°$. Ideally, we expect $\alpha = 70.6°$ and $\beta = \gamma = 54.7°$, and the small deviation is due to the slight curvature of the left arm of the triangular structure caused by the initial oxidation of the (111) surface, which has a nonuniform growth rate near the

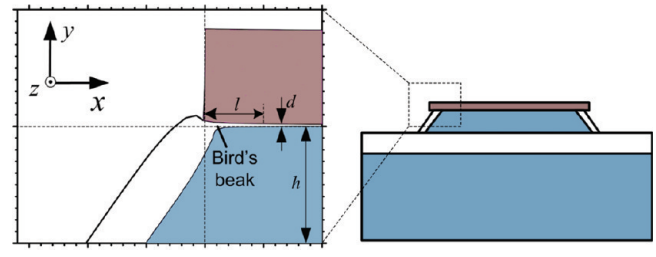

Figure 3. The local oxidation of silicon forms a protective region at the corner regions of the silicon mesa structure, allowing the precise formation of Si-NWs with arbitrary dimensions. Enlargement: graphical results of a two-dimensional finite element simulation (see Supporting Information) (blue, Si; white, SiO_2; brown, SiN).

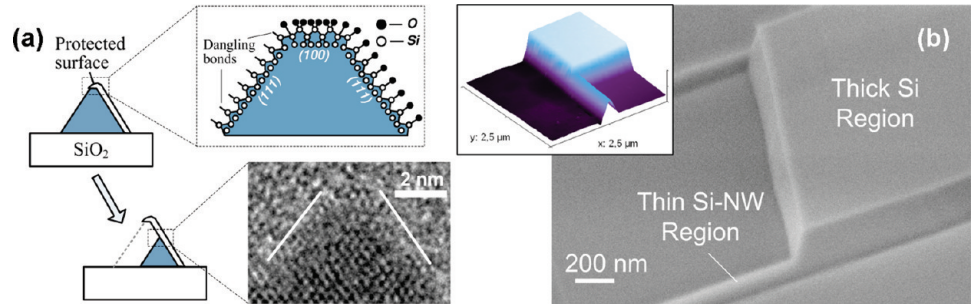

Figure 4. (a) Size reduction etching scheme. Upper right: Ideal atomic structure of the Si(111)/SiO_2 and Si(100)/SiO_2 interfaces (not to scale). Lower right: HRTEM of size reduced Si-NW apex. (b) HRSEM image of size reduced recessed Si-NWs showing interface between microscale electrical contact region and size reduced Si-NW from a continuous layer of silicon. Inset: TMAFM image.

sharp edges. These crystal plane inconsistencies are more pronounced as the Si-NW cross-section is made small ($h \approx 25$ nm in this case), and we have measured intersection angle deviations $\approx 1-2°$ for structures with $h \approx 100$ nm. Additionally, reducing the thickness of the thermal oxide or using in combination with a nonreactive oxide deposition can reduce the curvature of the (111) surface.

Electrical Characterization. The Si-NWs presented in this article are depletion-mode field-effect devices and have been realized with different dimensions and impurity-doping concentrations using SOI wafers. Measured data in Figure 5 show typical measured current−voltage ($I-V$) characteristics with and without back-gate biasing. Figure 5a shows a depletion effect[27,28] which requires $V_{ds} > 1$ V to open the Si-NW body channel allowing current to flow between the source and drain terminals with $V_{bg} = 0$ V. We attribute this channel depletion effect to fixed electronic charge located in the front oxide near the top silicon device layer surface Q_{f_fo} and in the buried oxide near the bottom of the silicon device layer Q_{f_bo} due to the reactive thermal oxidation of the silicon surfaces (Figure 5a). The fixed oxide charge is known to be positive and located near the Si/SiO_2 interface.[29] For p-type silicon, these fixed positive charges cause hole depletion in the silicon layer near the interface such that charge neutrality requires a negative charge in the silicon, which is pro-

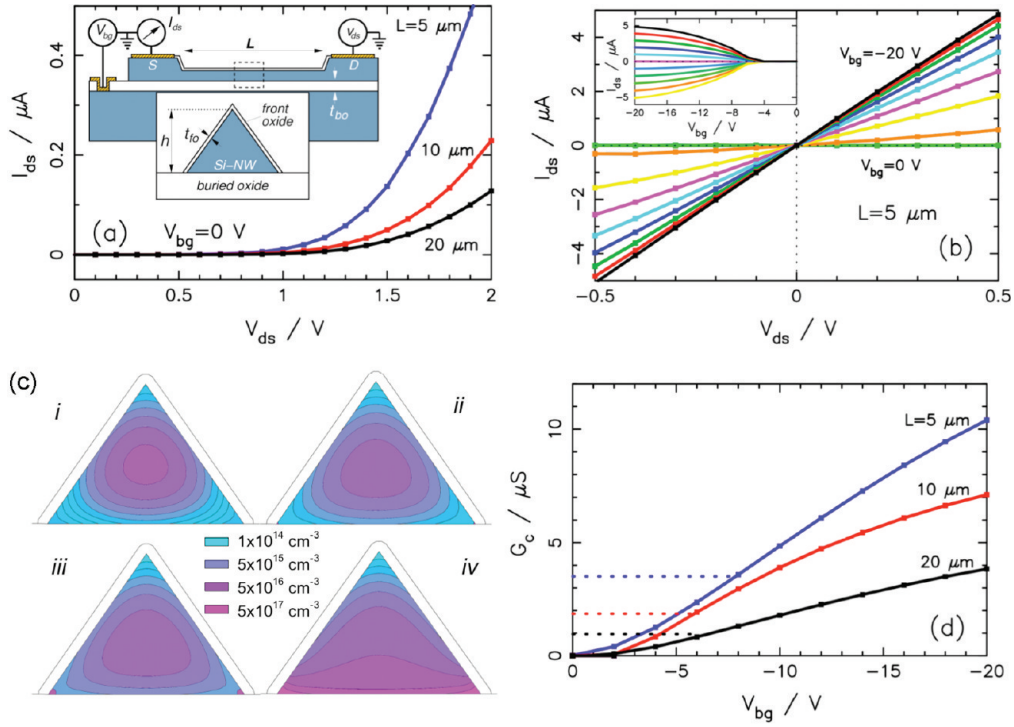

Figure 5. Measured Si-NW electrical characteristics (device height, $h = 140$ nm). (a) I_{ds} as a function of V_{ds} with $V_{bg} = 0$ V for devices with lengths $L = 5$ (blue), 10 (red), and 20 μm (black). (b) I_{ds} as a function of V_{ds} with -20 V $\leq V_{bg} \leq 0$ V in steps of 2 V. Inset: symmetric response as a function of V_{bg} for several V_{ds} values. (c) Calculated hole concentration in a Si-NW cross-section as V_{bg} is increased negatively (i−iv) using a two-dimensional finite element simulation with $Q_{f\_fo} = 2 \times 10^{11}$ cm^{-2}, $Q_{f\_bo} = 5 \times 10^{11}$ cm^{-2}, $N_a = 10^{17}$ cm^{-3} (uniform), $t_{fo} = 10$ nm and $t_{bo} = 100$ nm with the back-gate electrode located on the bottom edge of the buried oxide layer. (d) Measured channel conductance. Dashed lines represent ideal channel conductance for each length assuming $N_a = 1.6 \times 10^{17}$ cm^{-3}, $\mu_h = 284$ cm^2 V^{-1} s^{-1}, and $w_d = 50$ nm.

vided by the ionized impurities of a depletion region $Q_f \approx N_a w_d$, where N_a is the impurity concentration and w_d is the depletion width. Applying a negative potential across the interface using V_{bg}, with respect to V_{ds}, reduces the extent w_d, and therefore, the channel becomes partially depleted and results in linear $I-V$ characteristics for all values of V_{ds} (Figure 5b). Figure 5c shows how the partially depleted region increases as V_{bg} increases negatively from plot i to plot iv (back-gate electrode is symmetrically located on the bottom of the buried oxide layer), showing the results of two-dimensional finite element simulations (Taurus Medici, Synopsys). It should be noted that the maximum depletion width for a silicon layer doped with $N_a \approx 10^{17}$ cm^{-3}, is $w_d \approx 100$ nm which can easily deplete the NW device of majority of carriers when all three interfaces are considered. As V_{bg} is increased negatively the nondepleted region becomes larger compared to the depleted region. The last contour plot shows the largest nondepleted region, which includes the formation of a hole accumulation layer in the silicon layer near the interface that explains large measured channel conductances for large negative V_{bg} (Figure 5d).

The channel conductance can be estimated as $G_c = (\mu_h|Q_c| - \mu_h|Q_d| + \mu_{eff}|Q_a|)L^{-1}$, where Q_c (C cm^{-1}) is the hole channel charge per unit length, Q_d is the depletion charge, Q_a is the accumulation charge (for a p-type material $Q_c > 0$, $Q_d < 0$, and $Q_a > 0$), and μ_{eff} is the field-effect hole mobility in the accumulation region. On the basis of measured device dimensions (with TMAFM), the channel conductances of nondepleted Si-NWs with uniform doping concentration $N_a \approx 1.6 \times 10^{17}$ cm^{-3} (see Supporting Information), $h = 140$ nm, and $L = 5$, 10, and 20 μm are $G_c \approx 3.5$, 1.8, and 0.9 μS, respectively (dashed lines in Figure 5c), which are an upper limit for a nondepleted cross-section since the bulk hole mobility value is used and interface effects are not considered. Figure 5d shows the measured conductances as a function of V_{bg}. For $V_{bg} \approx -8$, -6, and -6 V the measured conductance matches the estimated conductance of nondepleted Si-NWs of each length, respectively. For $V_{bg} = -20$ V, the measured conductance increased to $G_c \approx 10$, 7, and 4 μS, well beyond the estimated conductance.

From calculations in Figure 5c and measurements in Figure 5d, it is clear that the addition of the accumulation charge contributes to the increased channel conductance beyond the estimated upper conductance limit for nondepleted structures. The estimation of carrier mobility in the NW is beyond the scope of this article and requires a model that takes into account the exact geometry of the back-gate contact and other device features. Additionally, measured $I-V$ characteristics of silicon microwires, 200 nm thick and 4 μm wide, are linear over the entire V_{ds} range and have conductances $G_c \approx 27$, 21, and 8 μS for lengths $L = 13$, 18, and 48 μm, respectively, and have a high correlation with conductance estimations with $\mu_h = 284$ cm^2 V^{-1}s^{-1}, $N_a = 1.6 \times 10^{17}$ cm^{-3}, and $w_d = 50$ nm. This discussion highlights the importance of the three-dimensional shape of nanostructures with respect to surface and interface effects due to the large surface to volume ratio (see Supporting Information).

The Si/SiO_2 interface states are also important and have not been included in the previous discussion due to the moderately high doping and cross-sectional area of the present devices. For lower doping levels ($\sim 10^{16}$) and smaller lateral dimensions ($\sim$20 nm) typical interface state densities $D_{it}^{(100)} \approx 10^{10}$ and $D_{it}^{(111)} \approx 10^{11}$ cm^{-2} eV^{-1},[30] which are amphoteric, can deplete the structure of all majority carriers and must be considered.[31,32]

For all electrical calculations the electrical contact resistance has been taken into account from extensive characterization using dedicated structures based on the transfer length method (TLM)[18] to extract the specific contact resistivity $\rho_c \approx 7 \times 10^{-4}$ Ω cm^{-2}. Measurements show quantitative agreement with reported values for sintered Al contacts on B-doped silicon with $N_a \approx 10^{17}$ cm^{-3}.[33] Contact resistivity $\sim 10^{-6}$ Ω cm^{-2} can be easily achieved by increasing the contact doping concentration; however, for all Si-NW devices tested the contact resistance contributes to less than 1% of the total electrical resistance.

Electrochemical Characterization. The electrochemical behavior of the depletion-mode p-type devices is demonstrated by measuring the current response of three different gate oxide configurations to varying pH of an electrolyte solution. The three oxide configurations include a SiO_2 gate oxide surface and oxide surfaces modified with organic monolayers 3-aminopropyltriethoxysilane (APTES) and hexamethyldisilazane (HMDS).

An oxide surface in contact with an aqueous solution is hydrated to form silanol (SiOH) surface molecules. The free-silanol groups on the oxide surface are acidic in nature according to $SiOH \leftrightarrow SiO^- + H^+$ with $pK_a \approx 6.8$.[34] The oxide surface may be positively charged, negatively charged or neutral depending on the pH of the electrolyte solution and the total oxide surface charge depends on the surface composition, crystal orientation and degree of hydration. Assuming that only hydroxyl groups (OH) react with the electrolyte, the oxide surfaces in solution can be described by the site-binding model (SBM),[35] which uses proton dissociation and association constants and the number of reactive sites on the oxide surface to describe the relationship between solution pH and surface potential ψ. The SBM has been used extensively to describe ion-sensitive field effect transistor sensors with

$$2.3(pH_{pzc} - pH) = \frac{\Psi}{kT} + \sinh^{-1}\left(\frac{\Psi}{\beta kT}\right)$$

where pH_{pzc} is the solution pH, $\psi \approx 0$, $\beta = q^2 N_s \delta/(C_{eq} kT)$ is a dimensionless sensitivity parameter, N_s the total

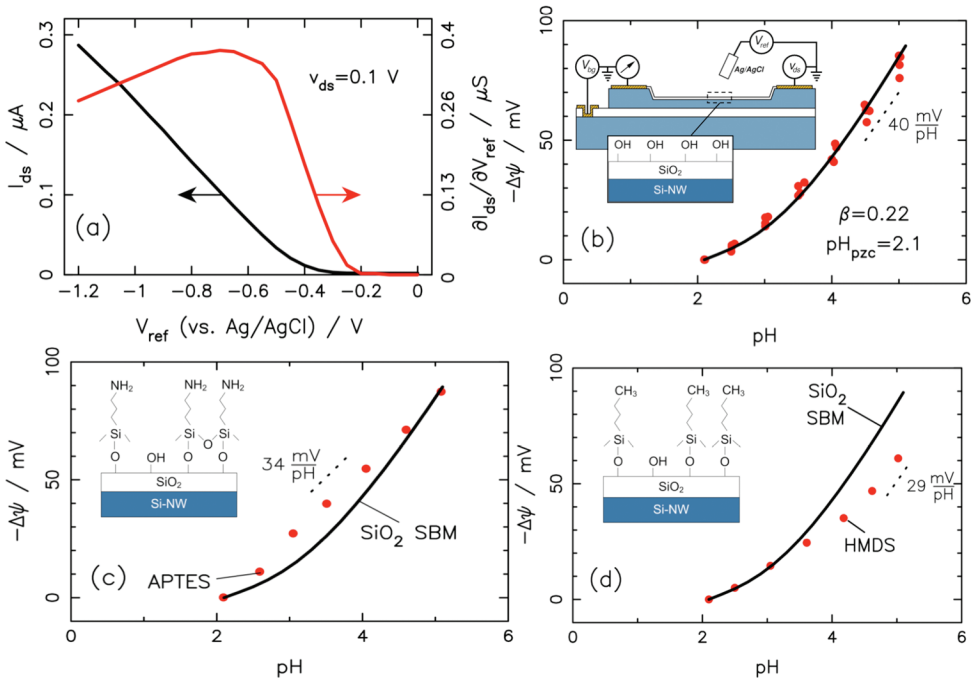

Figure 6. Measured electrochemical characteristics. (a)I_{ds} as a function of V_{ref} (V_{bg} = 0 V) in 100 mM NaCl (black) for fixed V_{ds} and $\partial I_{ds}/\partial V_{ref}$ as a function of V_{ref} (red). (b) pH behavior of oxidized Si-NWs in 100 mM NaCl titrated with HCl/NaOH. Solid line represents the SBM with β = 0.22 and pH_{pzc} = 2.1. (c) pH behavior of oxide surfaces modified with APTES organic monolayer. (d) pH behavior of oxide surfaces modified with an HMDS organic monolayer.

number of surface sites, δ is a measure of surface reactivity, and C_{eq} is the equivalent capacitance of the electric double-layer.[36]

Additionally, organic monolayers have been covalently conjugated to the oxide surface to demonstrate molecular gating of the NW current. An APTES monolayer attached to the oxide surface results in a mixture of hydroxyl and amine (NH_2) functional groups. The amine group is a base according to $R-NH_3^+ + H_2O \leftrightarrow R-NH_2 + H_3O^-$ with $pK_a \approx 9$.[37] Therefore, for solution pH below 7 the amine groups are mostly positively charged, which acts to increase the depletion layer width and reduce device current. The HMDS monolayer results in a mixture of surface of hydoxyl and methyl (CH_3) groups. The methyl group is nonpolar and does not react with the hydrogen ions in solution for pH ranges in this article. Therefore, the methyl groups act as surface site blockers that reduce N_s, and therefore, the pH sensitivity of the oxide surface.

A reference electrode is used as a front gate to bias the Si-NWs in solution for all surface charge related measurements. Front gate biasing affects the depletion region differently than back-gate biasing as presented previously and we expect higher surface charge sensitivity for biosensing applications with this configuration. Front gate conductivity modulation with a reference electrode (Ag/AgCl) in an electrolyte (100 mM NaCl) and corresponding transconductance ($\partial I_{ds}/\partial V_{ref}$, constant V_{ds}) illustrate the transition from depletion mode to depletion/accumulation mode operation as V_{ref} is scanned negative (Figure 6a). The decrease in transconductance for increasing V_{ref} is due to a decrease in field-dependent effective mobility and charge screening. For biosensing applications, the devices can be biased in the region with highest transconductance and linear I_{ds} range.[18] Figure 6b shows the measured Δψ-pH behavior of a representative Si-NW with a 10 nm thick gate oxide in NaCl electrolyte, where Δψ is the incremental change in surface potential. The SBM with β = 0.22 and pH_{pzc} = 2.1 is plotted with a solid black line, which shows a high correlation to the measured data. The sensitivity of 40 mV/pH from pH 4 to 5 is typical for oxide surfaces; however, the extracted sensitivity parameter is larger than typically reported.[36]

Figure 6 panels c and d show the measured pH behavior of oxidized Si-NW surfaces modified with organic monolayers APTES and HMDS. For APTES-modified oxide surfaces the amine functional groups are protonated at low pH resulting in a positive surface charge NH_3^+ and the hydroxyl groups are deprotonated at higher pH levels resulting in the negative surface charge O^-; the positive surface charge at low pH compensates for the nonlinear behavior of the bare oxide and results in a linear pH-ψ behavior and slightly lower pH sensitivity. For HMDS-modified surfaces, many of the surface hydroxyl ions are replaced with the organic monolayer with the nonpolar methyl functional group, which results in a ~28% reduction in pH sensitivity of the oxide surface (Figure 6d).

These measurements show that the new size reduced recessed Si-NW devices provide high quality Si-NW devices with precise doping concentrations, high quality electrical contacts, and stable operation, which are all critical for biosensing applications.

CONCLUSIONS

A new scalable Si-NW fabrication technology has been developed, based on a combination of conventional microfabrication steps that does not require expensive nanolithography to form sub-30 nm feature sizes. The advantage of this technology is that moderately dense arrays of Si-NWs, with precisely controlled dimensions and atomically smooth surfaces, are directly and simultaneously fabricated

with thick microscale electrical contact regions from a continuous layer of single crystal silicon using a novel size reduction method. Si-NW device arrays with lateral dimensions down to 10−20 nm and lengths up to 100 μm can be consistently fabricated with high wafer-level yields. Our simple Si-NW fabrication technology can be manufactured in any conventional microfabrication cleanroom.

METHODS

Silicon Nanowire Fabrication. Two types of commercial SOI substrates have been used, including silicon implanted with oxygen (SIMOX, Ibis, Inc., U.S.A.; Si DL, 200 nm; BOX, 150 nm) and UNIBOND (SOITEC, Bernin, France; Si DL, 200 nm; BOX, 400 nm). The silicon device layer is implanted with BF_2^+ ions (energy, 30 keV; dose, 10^{13} cm^{-2}; and angle, 7°). The thermal annealing steps for dopant activation and redistribution are distributed throughout the fabrication process. A thin low-stress SiN layer is deposited onto the silicon device layer by low-pressure chemical vapor deposition. The thin (<100 nm) low-stress SiN layer is required to prevent the formation of dislocations in the silicon layer due to stress generated by the volume expansion of the silicon dioxide layer during thermal oxidation. The first lithography mask is aligned to the wafer flat (see Supporting Information, Figure S1), and the SiN layer is patterned and selectively removed with reactive-ion etching (RIE). Lithography alignment errors are less than 1°. The [110] crystalline planes are aligned to the wafer flat within ±0.5° (see Supporting Information). The exposed silicon is then etched in a dilute tetramethyl ammonium hydroxide (TMAH, 5%; $C_4H_{13}NO$) etching solution. The local oxidation is done in a dry environment (950 °C, 15 min). The second lithography step is used to pattern and etch a 50-nm-thick layer of LPCVD polycrystalline silicon (polysilicon). The conformal polysilicon etch mask is critical for effectively masking the SiN etch without damaging the Si-NW surfaces. The SiN layer is then selectively removed using hot phosphoric acid (85% H_3PO_4, 180 °C) and later the polysilicon layer is removed. A second PDE step (TMAH 5%, 60 °C) forms the triangular Si-NWs. For applications requiring a gate dielectric, a thin oxide layer (10−20 nm) is grown on the (111) surfaces, which in all cases results in a rounded tip of the triangular Si-NW. The wafer is then annealed in an N_2 atmosphere (900 °C, 30 min) forming a uniform doping concentration, electrically activating the dopants and minimizing the fixed charge in the oxide layer. For electronic devices, two additional lithography steps are required to form electrical contact regions to the Si-NWs and substrate. A 400-nm layer of Al is deposited (preceded by the removal of the native oxide on the silicon surface with a buffered hydrofluoric acid wet etch) on the contact regions and annealed (400 °C, 20 min and 5% H_2 in N_2) to form good contact between the silicon and the metal layers. It should be noted that for p-type (*e.g.*, B) devices and contact regions, ohmic contacts can be formed with doping levels as low as ~10^{17} cm^{-3} when Al and subsequent annealing is used. The low temperature hydrogen anneal also reduces the interface state density D_{it} at the SiO_2/Si interface.

Surface Modification. Following wire bonding and encapsulation the oxide surface of the Si-NW prepared for electrochemical measurements. Prior to all experiments, the oxide surfaces are cleaned. Bare SiO_2 surfaces: the oxide surface was cleaned in UV ozone reactor for 3 min. HMDS modification: following oxide surface cleaning, the chip was immersed in pure hexamethyldisilizane at 60° F for 1 h and subsequently dried with dry nitrogen. APTES modification: following oxide surface cleaning, the chip was immersed in an 1% 3-aminopropyltriethoxysilane and 5% DI H_2O−ethanol solution for 30 min. The surface was washed with ethanol three times and dried in a convection oven at 120° for 5 min.

Electrical Measurements. Electrical measurements in air were recorded on a probe station (PM8, Karl Süss) using two source-measure units (2400, Keithley), one for the drain-source voltage (V_{ds}) and the second to sweep the back-gate contact voltage (V_{bg}). The source-measure units are controlled with the LabTracer2.0 software (Keithley).

Electrochemical Measurements. Si-NW devices were first encapsulated with a polyimide layer (thickness: 1 μm), followed by wire-bonding to a custom printed circuit board and finally all electrical wires and contacts were sealed with an epoxy (Hysol, Henkel Corporation). Following encapsulation, the Si-NW oxide surfaces were cleaned with UV ozone. Prior to electrochemical measurements the Si-NW devices were immersed in 100 mM NaCl at pH 2.1 for approximately 2 h for the electrolyte/SiO_2 interface to stabilize. The Si-NW device current was measured with a lock-in amplifier (SR830, Stanford Research Systems) with v_{ds} = 500 mV, 30 Hz modulation frequency, and V_{bg} = 0. A calibration curve was recorded by measuring the drain current response as the reference electrode (REF[200] Ag/AgCl, Radiometer Analytical) gate voltage was swept from $-2\ V \leq V_{ref} \leq 0\ V$. Following device calibration, the device current was recorded as the pH was increased from 2 to 5 in increments of 0.5. The measured $\Delta\psi$-pH was then calculated using the calibration curve.

HRTEM Sample Preparation and Imaging. Si-NW samples were prepared by depositing a 100 nm thick SiN protection layer onto the upper surface. The sample slices we prepared in a dual-beam FIB (FEI Tecnai G2 F20 X-Twin FEG TEM, Maser Engineering, Enschede, The Netherlands) and transferred to a TEM imaging grid. TEM imaging (FEI 3D-Strata DB-FIB FEG, Maser Engineering, Enschede, The Netherlands) was operated at 200 kV acceleration voltage.

AFM Imaging. A Digital Instruments Dimension 3100 was used for all AFM images. All AFM images performed in tapping mode with ultra sharp (average tip diameter ≈ 2 nm) single crystal silicon tips (SSH-NCH-10, NanoandMore, Gmbh).

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Supporting Information Available: Supporting Information includes details for photolithographic alignment to the [110] direction of (100) silicon wafers, plane dependent etching, local oxidation calculations and finite element simulation results, details of size reduction etching including a graph of etch rates and AFM and SEM images, description of selective ion-implantation and electrical characterization and estimation of the doping concentration in microscale devices. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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